CLAIMS

What is claimed is:

1. A jogging structure for translating wiring connections from points in a first grid to corresponding points in a second grid in a chip carrier module, the structure comprising:

a first translation layer, coupled to the first grid, said first translation layer translating the first grid in an x-axis direction; and

a second translation layer, coupled to said first translation layer, said second translation layer for translating said wiring connections from the first grid in a y-axis direction, said y-axis direction being orthogonal to said x-axis direction;

wherein said second translation layer is further coupled to the second grid.

2. The structure of claim 1, wherein:

the points within the first grid have a first pitch, said first pitch being defined by a first distance between neighboring points in the first grid;

the points within the second grid have a second pitch, said second pitch being defined by a second distance between neighboring points in the second grid; and

said second pitch is not an integral multiple of said first pitch.

3. The structure of claim 1, wherein:

said first translation layer further comprises a first plurality of signal interconnects, said first plurality of signal interconnects each having a jog line elongated along said x-axis direction; and

said second translation layer further comprises a second plurality of signal interconnects, said second plurality of signal interconnects each having a jog line elongated along said y-axis direction.

4. The structure of claim 3, wherein:

each of said jog lines in said first plurality of signal interconnects is disposed between an upper via contact and a lower via contact in said first translation layer; and

each of said jog lines in said second plurality of signal interconnects is disposed between an upper via contact and a lower via contact in said second translation layer.

5. The structure of claim 4, wherein:

each individual upper via contact in said first translation layer is in electrical communication with a corresponding point in the first grid;

each individual lower via contact in said first translation layer is in electrical communication with a corresponding upper via contact in said second translation layer; and

each individual lower via contact in said second translation layer is in electrical communication with a corresponding point in the second grid.
signal via in said first plurality of signal vias are in electrical contact with corresponding individual signal vias in said second plurality of signal vias.

6. The structure of claim 5, further comprising:

a first plurality of power busses in said first translation layer, disposed along said x-axis direction; and

a second plurality of power busses in said second translation layer, disposed in said y-axis direction.

7. The structure of claim 1, wherein:

the first grid comprises a C4 grid; and

the second grid comprises a logic service terminal (LST) grid.

8. A module for an integrated circuit (IC) chip, the module comprising:

a first grid for receiving electrical connections from the IC chip; and

a redistribution layer for fanning said electrical connections received by said first grid from said first grid to a second grid, said redistribution layer further comprising:

a first translation layer, coupled to said first grid, said first translation layer translating said first grid in an x-axis direction; and

a second translation layer, coupled to said first translation layer, said second translation layer for translating said wiring connections from said first grid in a y-axis direction, said y-axis direction being orthogonal to said x-axis direction;

wherein said second translation layer is further coupled to said second grid.

9. The module of claim 8, wherein:

the points within said first grid have a first pitch, said first pitch being defined by a first distance between neighboring points in said first grid;

the points within said second grid have a second pitch, said second pitch being defined by a second distance between neighboring points in said second grid; and

said second pitch is not an integral multiple of said first pitch.

10. The module of claim 8, wherein:

said first translation layer further comprises a first plurality of signal interconnects, said first plurality of signal interconnects each having a jog line elongated along said x-axis direction; and

said second translation layer further comprises a second plurality of signal interconnects, said second plurality of signal interconnects each having a jog line elongated along said y-axis direction.

11. The module of claim 10, wherein:

each of said jog lines in said first plurality of signal interconnects is disposed between an upper via contact and a lower via contact in said first translation layer; and

each of said jog lines in said second plurality of signal interconnects is disposed between an upper via contact and a lower via contact in said second translation layer.

12. The module of claim 11, wherein:

each individual upper via contact in said first translation layer is in electrical communication with a corresponding point in the first grid;

each individual lower via contact in said first translation layer is in electrical communication with a corresponding upper via contact in said second translation layer; and

each individual lower via contact in said second translation layer is in electrical communication with a corresponding point in the second grid.

13. The module of claim 12, further comprising:

a first plurality of power busses in said first translation layer, disposed along said x-axis direction; and

a second plurality of power busses in said second translation layer, disposed in said y-axis direction.

14. The module of claim 8, wherein:

said first grid comprises a C4 grid; and

said second grid comprises a logic service terminal (LST) grid.

15. A method for implementing a wiring translation in chip carrier module between corresponding points in a first grid and a second grid, the points in the first grid defining a first plane and the points in the second grid defining a second plane, the second plane lying substantially parallel to the first plane, the method comprising:

connecting the first grid to a first translation layer within the module, said first translation layer translating the points in the first grid in a first direction; and

connecting a second translation layer between said first translation layer and the second grid, said second translation layer translating the points in the first grid in a second direction, said second direction being orthogonal to said first direction.

16. The method of claim 15, wherein:

said first translation layer is configured to include a first plurality of signal interconnects, said first plurality of signal interconnects each having a jog line elongated along said x-axis direction; and

said second translation layer is configured to include a second plurality of signal interconnects, said second plurality of signal interconnects each having a jog line elongated along said y-axis direction.

17. The method of claim 16, wherein:

each of said jog lines in said first plurality of signal interconnects is disposed between an upper via contact and a lower via contact in said first translation layer; and

each of said jog lines in said second plurality of signal interconnects is disposed between an upper via contact and a lower via contact in said second translation layer.

18. The method of claim 17, wherein:

each individual upper via contact in said first translation layer is in electrical communication with a corresponding point in the first grid;

each individual lower via contact in said first translation layer is in electrical communication with a corresponding upper via contact in said second translation layer; and

each individual lower via contact in said second translation layer is in electrical communication with a corresponding point in the second grid.
signal via in said first plurality of signal vias are in electrical contact with corresponding individual signal vias in said second plurality of signal vias.

19. The method of claim 18, further comprising:

configuring a first plurality of power busses in said first translation layer, disposed along said x-axis direction; and

configuring a second plurality of power busses in said second translation layer, disposed in said y-axis direction.

20. The method of claim 15, wherein:

said first grid comprises a C4 grid; and

said second grid comprises a logic service terminal (LST) grid.